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# Design of an Embedded Hardware Platform for Cell-Level Diagnostics in Commercial Battery Modules

**GABRIELE MARINI [1], ALESSANDRO COLOMBO [1,2], ANDREA LANUBILE [1], WILLIAM A. PAXTON [3], AND SIMONA ONORI [1] (Fellow, IEEE)**

[1]Department of Energy Science and Engineering, Stanford University, Stanford, CA 94305 USA
[2]Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, 20133 Milan, Italy
[3]Innovation and Engineering Center California, Volkswagen Group of America Inc., Belmont, CA 94002 USA

CORRESPONDING AUTHOR: SIMONA ONORI (e-mail: sonori@stanford.edu).

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*(Gabriele Marini and Alessandro Colombo contributed equally to this work.)*

**ABSTRACT** While battery aging is commonly studied at the cell-level, evaluating aging and performance within battery modules remains a critical challenge. Testing cells within fully assembled modules requires hardware solutions to access cell-level information without compromising module integrity. In this paper, we design and develop a hardware testing platform to monitor and control the internal cells of battery modules contained in the Audi e-tron battery pack. The testing is performed across all 36 modules of the pack. The platform integrates voltage sensors, balancing circuitry, and a micro-controller to enable safe, simultaneous cell screening without disassembling the modules. Using the proposed testing platform, cell voltage imbalances within each module are constrained to a defined reference value, and cell signals can be safely accessed, enabling accurate and non-invasive cell-level state-of-health assessments. On a broader scale, our solution allows for the quantification of internal heterogeneity within modules, providing valuable insights for both first- and second-life applications and supporting efficient battery pack maintenance and repurposing.

**INDEX TERMS** Embedded hardware, battery systems, Li-ion, module testing, balancing, monitoring.

## I. INTRODUCTION

The electric vehicle (EV) market has experienced exponential growth in recent years, and this trend is likely projected to continue as EVs play a crucial role in global decarbonization efforts [1]. This growth has driven significant advancements in lithium-ion batteries (LIBs), which are renowned for their long cycle life, high energy density, and low self-discharge rates [2]. These characteristics have made LIBs indispensable across various sectors other than transportation, such as consumer electronics, medical equipment, power tools, renewable energy storage systems and data centers [3].

LIB packs are arranged in modules, each comprising multiple cells connected electrically and thermally, and meeting high energy requirements requires a large population of interconnected components. Consequently, small cell-to-cell electrochemical differences can translate into non-homogeneous behavior (e.g., uneven current sharing among parallel-connected cells and voltage imbalance among series-connected cells) and can propagate from cell to module and pack, ultimately affecting pack performance and lifetime. For these reasons, internal pack screening and diagnostics are essential for assessing variability and ensuring reliable operation. Such screening can be performed either at the cell level or at the module/pack level [4], [5].

Heterogeneity characterization becomes even more critical for battery repurposing, i.e., when EV battery packs approaching the end of their service life are reused in less demanding second-life applications (e.g., commercial/industrial energy storage systems) [6], [7], [8], [9], where identifying

underperforming and close to failure components is key to enabling reliable battery reuse.

In the remainder of the paper, we adopt the *x*P*y*S notation to indicate the module/pack topology, where $x$ denotes the number of cells connected in parallel (to form a parallel array) and $y$ denotes the number of such parallel arrays connected in series. When either $x$ or $y$ equals 1, it is omitted.

The open literature reports module-level testing conducted either on laboratory-built modules or on commercially available systems. In the case of lab-built modules, small, low-voltage configurations (up to 5 V) composed of parallel-connected cells have attracted increasing attention. For example, [10] investigates the effects of thermal gradients on current distribution, while [11] analyzes their impact on cell degradation. In addition, [12] compares different module topologies to evaluate the effectiveness of air ventilation, and [13] examines thermal runaway propagation in parallel-connected cells. A number of studies focus on current imbalances in parallel configurations driven by multiple factors. In [14], current distribution is examined between $LiFePO_4$ and $Li(NiCoAl)O_2$ cells, while [15] proposes mitigating these imbalances through the introduction of a controllable interconnection resistance. Similarly, [16] models the impact of cell inconsistencies on current distribution and validates the approach on aged cells, whereas [17] investigates the influence of current-collector geometry and resistance. In [18], current imbalances and their impact on degradation are analyzed in a 2P array. [19] investigates capacity and resistance heterogeneities in a 4P module with Hall-sensor-based current measurements (dataset in [20]), while [21] uses Differential Voltage Analysis (DVA) to reveal imbalance effects on differential-voltage features. For series-connected cells, [13] investigates thermal-runaway propagation in a 9S module configuration, and [22] studies aging propagation in a 4S string. [23] introduces a fully instrumented, reconfigurable module (up to 8S/8P) to track current, voltage, and energy distributions over aging. Finally, [24] develops a 504-cell pack for a prototype EV and uses pack-level data for fault detection. In contrast, academic studies on commercially available battery modules are limited, primarily due to the need for high-voltage testing equipment. In [25], a screening method is proposed for a retired EV pack, although it does not resolve individual cell properties. [26] investigates modules from a Volkswagen ID.3 Pro Performance pack, where cell-level data are obtained through irreversible disassembly, followed by individual cell testing within the module casing to preserve mechanical and thermal conditions. Similarly, [27] analyzes modules from a Mercedes-Benz Vito e-Cell pack via accelerated module-level aging and periodic cell-level reference tests, requiring repeated disassembly and reassembly. [28] conducts accelerated aging tests at the module and pack levels using modules manufactured by Lishen Battery Company Ltd. to develop a state-of-health (SOH) estimator. Overall, these studies rely on module disassembly to access cell-level signals. To date, the only openly reported example enabling non-destructive internal module access is the Nissan Leaf 2P2S module, which incorporates a third terminal providing direct electrical access to each 2P block [29], [30], [31]. To the best of the authors' knowledge, a non-disruptive hardware platform for cell-level screening of series-connected cells within commercial modules is still unavailable. This work addresses this gap by introducing a custom-designed, low-power embedded system capable of non-invasively measuring individual cell voltages without opening the module casing. The platform also integrates cell balancing functionalities to enhance safety and reliability. Building on these measurements, we propose a methodology to quantify cell heterogeneities in terms of capacity, energy, and resistance. The paper is organized as follows: Section II presents the experimental setup; Section III details the methodology for extracting cell-level metrics; Section IV reports the analysis across all cells; and Section V concludes the paper.

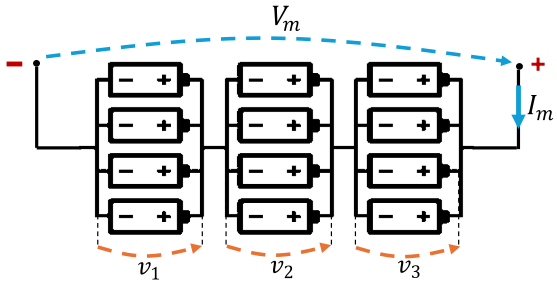


**FIGURE 1.** Schematic 4P3S topology; $v_1$, $v_2$, $v_3$ are the *Cells* terminal voltage; $I_m$ module current; $V_m$ module voltage.

## II. EXPERIMENTAL SETUP AND DESIGN

This section is organized as follows: module configuration, battery cycling equipment, embedded monitoring and balancing circuitry, and testing profile design.

### A. MODULE CONFIGURATION

This study is based on modules from a 95 kWh battery pack from an all-electric Audi e-tron. The vehicle was driven in the San Francisco Bay Area, CA, from September 2021 through January 2024, after which the pack was disassembled at the VW North America facility in Belmont, CA. Individual modules were extracted and then tested one by one in the Stanford Energy Control Laboratory, Stanford University [32] from February through May 2024. The pack consists of 36 modules connected in series, each consisting of 12 NMC pouch cells arranged in a 4P3S configuration, as shown in Fig. 1. In this work, each 4P group is represented as a single lumped element, denoted as *Cell*, since the parallel-connected cells share the same terminal voltage and individual currents are not accessible. Each module comprises three *Cells*, for a total of 108 *Cells* in the pack. Each *Cell* carries the module current $I_m$. Each module is equipped with external connectors (G-, C1+, C2+, and C3+, see Fig. 2), whose potential differences provide the *Cell* terminal voltages, denoted as $v_j$, $j \in \{1, 2, 3\}$. Battery specifications in terms of rated voltage, capacity and

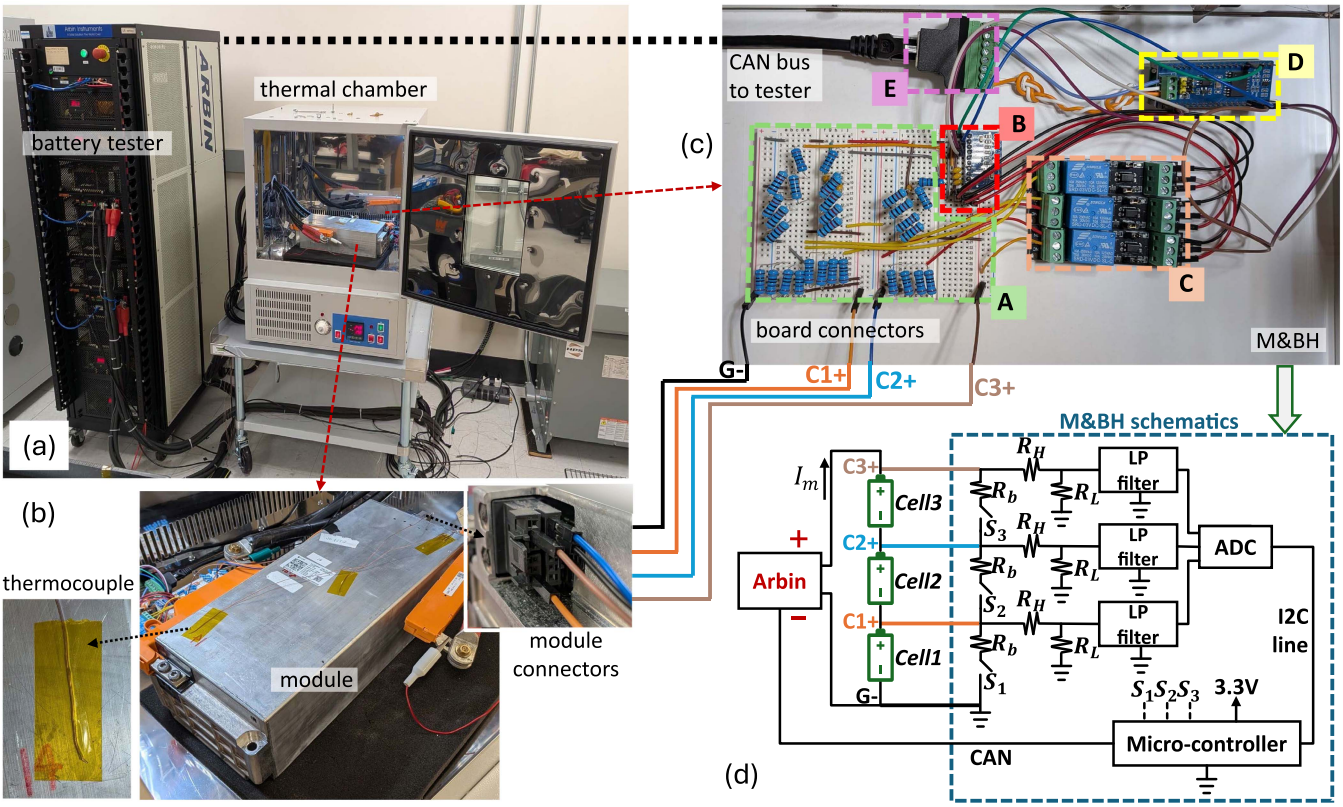


**FIGURE 2.** (a) Battery tester and thermal chamber with the module mounted inside; (b) detailed view of the module, including external connectors and thermocouple placement (three thermocouples attached to the module casing); (c) components of the M&BH: (A) analog electrical circuit, (B) ADC, (C) balancing switches, (D) microcontroller, and (E) CAN adapter for the cycler; (d) schematic of the overall setup, including the battery tester, the module (series-connected *Cells*), and the M&BH. The module-to-board connections are highlighted with different colors: G− (black) is the module ground, C1+ (orange), C2+ (blue), and C3+ (brown) are the *Cell* positive terminals.

**TABLE 1.** Battery Cell, *Cell*, Module and Pack Specifications

| | Rated voltage [V] | Rated capacity [Ah] | Rated energy [kWh] |
|---|---|---|---|
| cell | 3.6 | 61.2 | 0.22 |
| *Cell* (4P) | 3.6 | 244.8 | 0.88 |
| module (4P3S) | 10.8 | 244.8 | 2.64 |
| pack (4P108S) | 388.8 | 244.8 | 95.04 |

energy are summarized in Table 1. Physical cell specifications are taken from the datasheet, whereas *Cell*, module, and pack specifications are derived from the electrical topology. The cells operate within a voltage window of $v_{\min} = 3.3$ V and $v_{\max} = 4.2$ V, respectively, which directly translates to a module voltage range of [9.9, 12.6] V and pack voltage range of [356.4, 453.6] V.

### B. BATTERY CYCLER AND THERMAL CHAMBER

The laboratory setup for module testing is illustrated in Fig. 2(a). An Arbin LBT22013 battery cycler is used for test actuation, with modules placed inside an Amerex IC150R thermal chamber to maintain a controlled ambient temperature. Surface temperature is monitored via three thermocouples attached to the module casing (Fig. 2(b)). A safety cutoff is enforced to terminate the test if any thermocouple exceeds 50 °C. The three measurements are consistent (see Appendix III), and the module temperature is defined as their average. The Arbin system records the module current and voltage.

### C. ELECTRONIC CIRCUIT DESIGN

To monitor internal voltages without opening or altering the module casing, a dedicated electronic board, referred to as the Monitoring and Balancing Hardware (M&BH), is developed. The hardware, shown in Fig. 2(c) with schematic in Fig. 2(d), comprises:

A) a board featuring an analog electrical circuit composed of a resistor/capacitor (RC) network;
B) an analog-to-digital converter (ADC);
C) balancing switches;
D) a micro-controller;
E) a CAN adapter for communication to/from the cycler.

The parameter values for the analog circuit are reported in Appendix I (Table 5). The tolerances on the values are ±1%. In the following, the M&BH features are described in detail.

#### 1) MEASURING THE *CELL* VOLTAGES

Voltage measurement is enabled by direct access to the *Cell*-level potentials through the module external connectors (Fig. 2(b)), which provide the positive terminal voltages (C1+, C2+, C3+) with respect to the common ground (G-). These signals are first scaled using voltage dividers with resistive pairs $R_H$ and $R_L$, which scale the potentials by a factor of $\frac{R_L}{R_H+R_L} = 0.25$ to match the ADC input range. The scaled voltages are then filtered by an analog low-pass RC filter with cutoff frequency $f_{LP} = 112.9$ Hz and subsequently digitized by an ADC (ADS1115) at a sampling rate of 10 Hz. This measurement pipeline follows standard BMS practice, where cell voltages are scaled through voltage dividers, filtered, and digitized [33], [34]. The microcontroller (Raspberry Pi Pico) then rescales the digitized signals to their original voltage range, reconstructs the corresponding *Cell* terminal voltages, and transmits them to the battery cycler via CAN at 10 Hz. Additional details on the voltage measurement pipeline are included in Appendix I.

The proposed platform is tailored to the considered module configuration comprising three *Cells*; however, it can be readily extended to modules with an arbitrary number of series-connected *Cells*. The requirement for external connectors providing cell-level potentials is not a limitation, as such connectors are standard in modern battery modules for BMS-based cell-level monitoring. While the connector type may vary across pack designs, the presented hardware can accommodate different standards through minor adaptations of the interface (e.g., replacing the pin connectors with alligator clips or other suitable connectors).

#### 2) CELL BALANCING

*Cell* balancing is used to mitigate voltage imbalances among *Cells*. If left unaddressed, such imbalances can lead to over or under charging, thermal gradients, and, ultimately, reduced performance and safety. The implemented balancing strategy is a standard passive balancing scheme [35], [36], in which excess charge from higher voltage *Cells* is dissipated through parallel branches containing bleeding resistors $R_b$. Each *Cell* is associated with a controllable switch connected in series with its corresponding resistor. For the $j$-th *Cell*, the switch state $S_j$ determines the balancing operation:

- $S_j = 0$ (open): the parallel branch of the $j$-th *Cell* is inactive, and the entire module current flows through the *Cell*;
- $S_j = 1$ (closed): part of the module current is diverted through the bleeding resistor, dissipating excess energy and activating balancing.

Each switch is independently controlled by the microcontroller based on the measured cell voltages. Given the binary nature of the switch position $S_j$, a threshold-based bang-bang balancing strategy is implemented. Since the objective is to limit voltage imbalances within each module, the control law for the $j$-th *Cell* is defined as:

$$S_j(v_1, v_2, v_3) = \begin{cases} 1, & \text{if } v_j \geq \min(v_1, v_2, v_3) + v_{th} \\ 0, & \text{otherwise} \end{cases}, \quad (1)$$

where $v_{th}$ is a predefined voltage threshold and $v_j$ is the voltage of the $j$-th *Cell*. The balancing switch is activated, $S_j = 1$, for those *Cells* whose voltage exceeds the minimum voltage within the triplet by more than $v_{th}$. As a result, no more than two switches can be closed simultaneously. After a balancing interval, the maximum voltage imbalance $\Delta v_{\max}$ among *Cells* aims not to exceed $v_{th}$:

$$\Delta v_{\max} = \max(v_1, v_2, v_3) - \min(v_1, v_2, v_3) \leq v_{th}. \quad (2)$$

The effectiveness of the balancing action depends on both the duration of the balancing phase and the initial value of $\Delta v_{\max}$. In particular, for larger initial imbalances, a short balancing duration may be insufficient to achieve the desired equalization. It is important to notice that voltage regulation indirectly enables control of each *Cell*'s state-of-charge (SOC) since higher *Cell* voltages correspond to higher SOC. By closing the balancing switch of an overcharged *Cell*, the current flowing through it is reduced, thereby lowering its charging rate. In this work, $v_{th}$ is set to 2.5 mV and the bleeding resistance is chosen as $R_b = 67.5\ \Omega$ consistent in order of magnitude with on-board values. The effect of the bleeding resistance on SOC dynamics is analyzed in Appendix II.

### D. TESTING PROFILE

Dedicated diagnostic tests were conducted to extract key aging-related metrics at the *Cell* level. Specifically, discharge capacity and discharge energy are computed from capacity tests; the internal resistance using Hybrid Pulse Power Characterization (HPPC) tests. Fig. 3 illustrates the designed module current profile, actuated using the Arbin cycler, along with the resulting module voltage. Additional details are provided below.

#### 1) CAPACITY TEST

The capacity test consists of a C/3 discharge, corresponding to a constant current of 81.6 A. The applied C-rate is configurable, depending on the application and time constraints. Starting from 12.6 V, the module is discharged until the *Cell* with the lowest voltage reaches the predefined lower threshold of 3.3 V (i.e., the cell cutoff voltage). This is followed by a one-hour rest period. Balancing is intentionally deactivated during this test as the resulting voltage imbalances at the end of discharge are required to quantify capacity heterogeneities among the *Cells*, as described in Section III. The test is conducted at a controlled chamber temperature of 25 °C.

#### 2) HPPC

The HPPC alternates C/3 discharges, one-hour resting intervals, and current pulses at different C-rates. It is conducted at

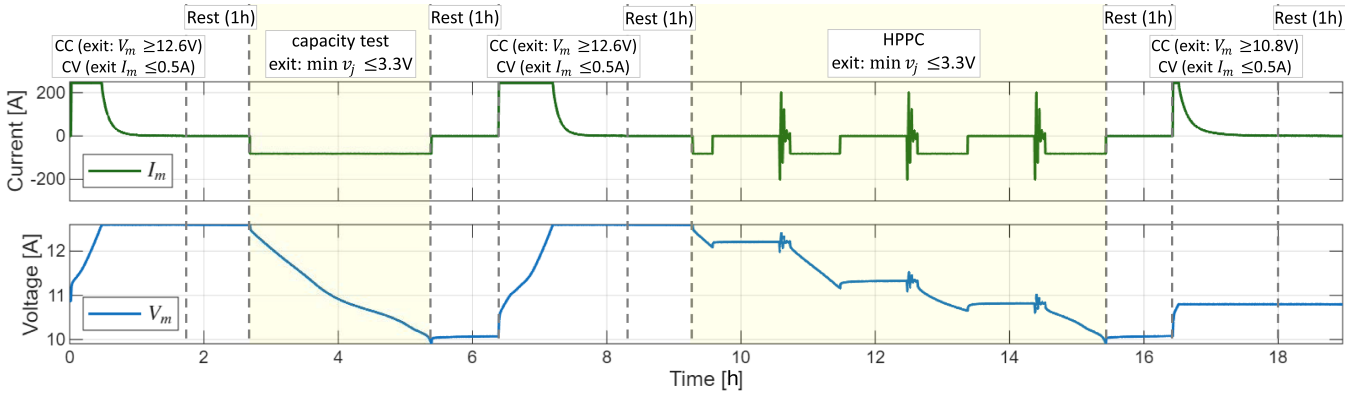


**FIGURE 3.** Top: actuated module current profile $I_m$. Bottom: resulting module voltage $V_m$ (for module no.29). The description and the exit conditions of each portion are reported; diagnostic segments are highlighted in yellow. By convention, positive current means charging; negative discharging.

three SOC levels, i.e. 90%, 65%, and 40%. These SOC levels are reached via Coulomb counting during a C/3 discharge, using the rated *Cells* capacity as a reference (see, Table 1). At each SOC level, a sequence of eight consecutive current pulses is applied, including 4/5 C (200 A), C/2 (122.4 A), C/10 (24.48 A), and C/20 (12.24 A), each performed in both discharge and charge. Each pulse lasts 15 s and is followed by a 60 s rest period. At the end of the protocol, the module is discharged until the cell with the lowest voltage reaches 3.3 V, followed by a one-hour rest period. Balancing is disabled throughout the HPPC test. All tests are conducted at three controlled temperatures, namely, 15 °C, 25 °C and 35 °C.

### 3) CC-CV CHARGING

Before the diagnostic tests, the module is charged at 244.8 A (1 C) constant current (CC) until its voltage reaches the upper cutoff value 12.6 V; after that, it is kept at constant voltage (CV) until the current decreases to 0.5 A (C/500). During the CC-CV phase, balancing is active, ensuring that all *Cells* reach the same voltage (4.2 V) at the start of the diagnostic tests, with a maximum deviation of 2.5 mV according to the implemented balancing strategy. The final CC–CV charge is instead used to restore the cells to their rated voltage at the end of the testing profile. Each CC–CV charging phase is followed by a one-hour rest period.

The resulting *Cell*-level signals for module no.29 are shown in Fig. 4. The balancing strategy described in (1), active during the CC-CV phases, effectively reduces voltage differences among the *Cells* and maintains them within the desired threshold.

## III. QUANTITATIVE METRICS COMPUTATION

This section presents the methodology used to compute the metrics from the proposed experimental setup.

### A. DISCHARGE CAPACITY

The discharge capacity of each *Cell* within a module is obtained from the capacity test via Coulomb counting, i.e., by integrating the module current over a fixed voltage range.

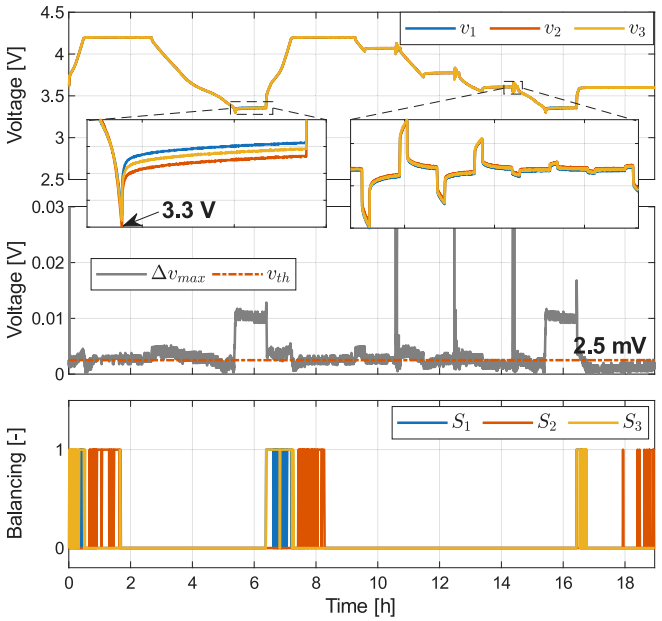


**FIGURE 4.** Top: measured *Cell* voltages $v_1$, $v_2$, $v_3$, with zoomed-in views. Middle: maximum *Cell* voltage imbalance $\Delta v_{max}$ and balancing threshold $v_{th}$. Bottom: switch states $S_1$, $S_2$, $S_3$ determined by (1).

Starting from a common initial voltage (4.2 V ± 2.5 mV), the final voltages of the *Cells* at the end of the test may differ due to capacity heterogeneities. In particular, the *Cell* with the lowest capacity depletes its SOC faster and reaches the lower cutoff voltage first. Quantifying discharge capacity over a common voltage range therefore provides a direct measure of capacity heterogeneity among the *Cells*. A visualization of the resulting voltage imbalances at the end of the capacity test is shown in Fig. 4 (zoom of the top plot, left).

Given the module current $I_m$ and a voltage window $[\underline{v}, \bar{v}]$, the discharge capacity $q_j$ of the $j$-th *Cell* is computed as

$$q_j = \frac{1}{3600} \int_{t_0 : v_j(t_0) = \bar{v}}^{t_f : v_j(t_f) = \underline{v}} |I_m(t)| \, \mathrm{d}t. \tag{3}$$

**Algorithm 1:** Voltage window $[\underline{v}, \bar{v}]$ iterative computation.

$\bar{v}^{(\mathbf{0})} \leftarrow v_{\max}$ ▷Initialize upper bound
$\underline{v}^{(\mathbf{0})} \leftarrow v_{\min}$ ▷Initialize lower bound
$h = 1$ ▷Initialize module counter
**while** $h \leq N_{modules} = 36$ **do** ▷Iterate over modules
  Execute testing profile on module $h$
  Extract the C/3 discharge voltage profiles $v_j(i)$, for $i = 1, \ldots, N_{samples}$ and for all $j = 1, \ldots, N_{Cells}$
  $j = 1$ ▷Initialize *Cell* counter
  **while** $j \leq N_{Cells} = 3$ **do** ▷Iterate over *Cells*
    $\bar{v}^{(\mathbf{h})} \leftarrow \min(\max_i v_j(i), \bar{v}^{(\mathbf{h-1})})$ ▷Update upper bound
    $\underline{v}^{(\mathbf{h})} \leftarrow \max(\min_i v_j(i), \underline{v}^{(\mathbf{h-1})})$ ▷Update lower bound
    $j \leftarrow j + 1$ ▷Increment *Cell* counter
  **end while**
  $h \leftarrow h + 1$ ▷Increment module counter
**end while**
$\bar{v} \leftarrow \bar{v}^{(\mathbf{h})}$ ▷Return upper bound
$\underline{v} \leftarrow \underline{v}^{(\mathbf{h})}$ ▷Return lower bound

The bounds $\bar{v}$ and $\underline{v}$ define the largest common voltage window across all *Cells*, during the C/3 capacity test.

Specifically, after testing all modules in the pack, $\bar{v}$ is set to the minimum of the initial voltages observed across all *Cells*, while $\underline{v}$ is defined as the maximum final voltage. The iterative procedure used to compute $[\underline{v}, \bar{v}]$ is described in Algorithm 1. This approach ensures a consistent *Cell* capacity comparison not only within individual modules but also across the entire battery pack. Algorithm 1 yields a slightly reduced voltage window, with $\underline{v} = 3.3373$ V and $\bar{v} = 4.1953$ V. The lower bound is about 37 mV above the lower cutoff voltage (3.3 V) reflecting discharge imbalance driven by capacity heterogeneities. The upper bound is about 5 mV below 4.2 V due to residual imbalances that persist despite the balancing algorithm, which may require longer balancing durations to fully converge within the ±2.5 mV threshold. In (3), the integral is normalized by 3600 to convert the integrated current into ampere-hours (Ah). Because all *Cells* carry the same module current, the module discharge capacity $Q_m$ is limited by the *Cell* with the lowest discharge capacity, namely,

$$Q_m = \min(q_1, q_2, q_3). \tag{4}$$

The *Cell* with the lowest capacity is referred to as the *weakest Cell*.

### B. DISCHARGE ENERGY

Similarly, the discharge energy $e_j$ of the $j$-th *Cell* test is obtained by integrating the power, i.e., $v_j(t)I_m(t)$, over the same voltage window:

$$e_j = \frac{1}{3600} \int_{t_0:v_j(t_0)=\bar{v}}^{t_f:v_j(t_f)=\underline{v}} \left| v_j(t)I_m(t) \right| \mathrm{d}t. \tag{5}$$

The voltage window is the one defined by Algorithm 1, and the integral is normalized by 3600 to express the discharge energy in watt-hours (Wh).

Since the module voltage is the sum of the *Cell* voltages, the module discharge energy $E_m$ is given by

$$E_m = \sum_{j \in 1,2,3} e_j. \tag{6}$$

The metrics in (5) and (6) include both the *Cells*' energy and the energy dissipated in the interconnect resistances due to the voltage measurement; nonetheless, the latter contribution is assumed negligible.

### C. INTERNAL RESISTANCE

The internal resistance of each *Cells* is estimated from the ohmic voltage drop induced by current pulses during the HPPC test. For each SOC level $SOC \in \{40\%, 65\%, 90\%\}$ and temperature $T \in \{15\ ^\circ\mathrm{C}, 25\ ^\circ\mathrm{C}, 35\ ^\circ\mathrm{C}\}$ (i.e., nine SOC–temperature combinations), the resistance $r_j$ of the $j$-th *Cell* is computed as the ratio between the instantaneous voltage drop and the corresponding current pulse amplitude, under the assumption of zero current prior to the pulse (by design). To improve robustness to noise, the resistance is averaged over all pulses applied at the same SOC level:

$$r_j = \frac{1000}{N_{pulses}} \sum_{h=1}^{N_{pulses}} \left| \frac{\Delta v_{j,h}}{I_{pulse,h}} \right|, \tag{7}$$

where $N_{pulses} = 8$, $I_{pulse,h}$ is the amplitude of the $h$-th pulse, and $\Delta v_{j,h}$ is the corresponding voltage drop. The factor 1000 converts the resistance to milli-ohms. A visualization of the ohmic voltage drops during the HPPC test is shown in Fig. 4 (top panel, zoomed view).

Internal resistance is an inherently instantaneous (pulse-based) metric and is therefore sensitive to acquisition latency and signal misalignment. In our setup (see Appendix I), the board-to-Arbin communication introduces an approximately 100 ms delay between the module current signal (measured directly by the Arbin) and the Cell voltage signals (measured by the electronic board and transmitted via CAN). As a result, the onset of the current pulse does not exactly coincide with the corresponding voltage drop (see Fig. 13). This misalignment is explicitly accounted for when computing $\Delta v_{j,h}$ in (7). Specifically, for each current pulse $h$, the voltage drop $\Delta v_{j,h}$ is evaluated by detecting the transition and computing the difference between the first voltage sample after the drop and the last sample before the drop.

Once the resistance values are computed for each SOC and temperature, a parabolic relationship between resistance $r$ and temperature $T$ is fitted to capture the observed inverse dependence between the two variables [37]. The model takes the following form:

$$r(T, SOC) = \frac{a_1(SOC)}{T - a_2(SOC)} + a_3(SOC), \tag{8}$$

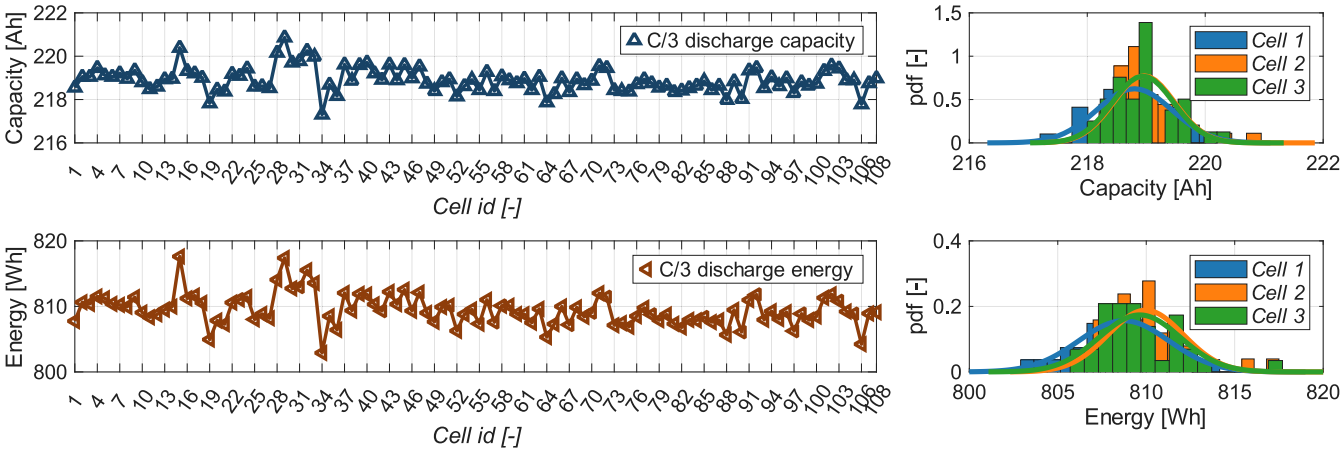


**FIGURE 5.** Top: C/3 discharge capacities for all 108 *Cells* in the pack. Bottom: corresponding C/3 discharge energies. Right: capacity and energy distributions by *Cell* position within each module, with Gaussian fits.

where the coefficients $\{a_m\}_{m=1,2,3}$ are SOC-dependent parameters.

## IV. EXPERIMENTAL RESULTS

This section presents the main results obtained from 36 modules tested. These results provide a comprehensive characterization of all the *Cells* of the pack and enable the identification of heterogeneities both within individual modules and across the entire pack.

### A. CAPACITY AND ENERGY HETEROGENEITIES

Fig. 5 shows the C/3 discharge capacities (top) and C/3 discharge energies (bottom) for all *Cells* in the pack, computed using (3), (5) and Algorithm 1. Each module test characterizes a set of three *Cells*. On the left-hand side, capacities and energies are plotted according to the *Cell* position within the pack (following the module ordering) highlighting intrinsic variations. The capacity and energy trends are consistent, with the lowest values observed for *Cell* no. 34. The spread of these values reflects the extent of heterogeneity across the pack. On the right-hand side, the distributions of discharge capacity and energy are shown as a function of the *Cell* position within each module. While the distributions are generally consistent across *Cells*, *Cell* 1 exhibits a slightly lower mean and higher variance compared to *Cells* 2 and 3, indicating marginally different behavior (also supported by Gaussian fits). The mean, standard deviation, minimum and maximum value of these distributions are listed in Table 2.

The corresponding module-level capacity and energy values are shown in Fig. 6, computed according to (4) and (6). On the left-hand side, discharge capacity and energy for all modules are reported, with their statistical properties summarized in Table 2. On the right-hand side, their correlation is shown, with a Pearson coefficient of $\rho = 0.924$, indicating a strong relationship between the two quantities. Notably, module no.12 exhibits the lowest capacity and energy, consistent with the fact that it contains *Cell* no.34, identified as the weakest *Cell* in the pack. A detailed look at the weakest *Cell*

**TABLE 2.** Discharge Capacity and Energy Statistics Based on the *Cell* Position Within the Module. Module-Level Stats are Reported as Well

| | mean [Ah] | std [Ah] | min [Ah] | max [Ah] |
|---|---|---|---|---|
| **C/3 discharge capacity** | | | | |
| *Cell* 1 | 218.80 | 0.64 | 217.31 | 220.16 |
| *Cell* 2 | 218.96 | 0.52 | 218.26 | 220.86 |
| *Cell* 3 | 218.95 | 0.52 | 218.03 | 220.39 |
| module-level | 218.58 | 0.49 | 217.31 | 219.78 |
| | **mean [Wh]** | **std [Wh]** | **min [Wh]** | **max [Wh]** |
| **C/3 discharge energy** | | | | |
| *Cell* 1 | 808.73 | 2.55 | 802.90 | 814.07 |
| *Cell* 2 | 809.97 | 2.12 | 807.31 | 817.40 |
| *Cell* 3 | 809.63 | 2.29 | 806.09 | 817.62 |
| module-level | 2428.33 | 5.90 | 2417.84 | 2444.22 |

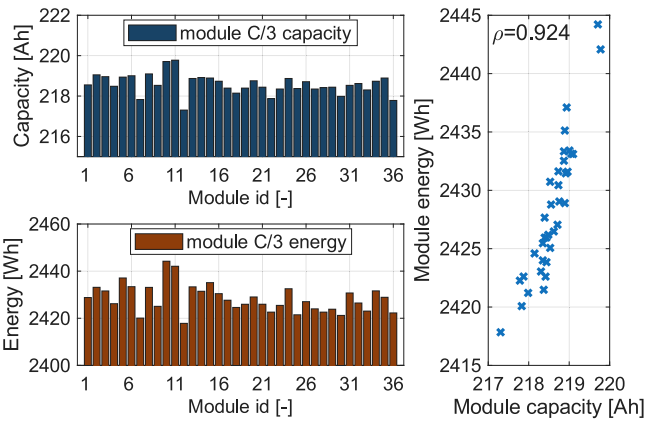


**FIGURE 6.** Left: module-level discharge capacity and energy. Right: correlation between capacity and energy.

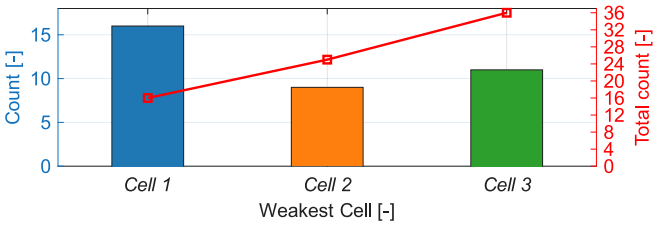


**FIGURE 7.** Histogram of the weakest *Cells* across the 36 modules. Left axis: occurrences of the weakest *Cell* across the three *Cells* of the module. Right axis: cumulative count of occurrences (up to 36).

within each module is shown in Fig. 7. *Cell* 1 is identified as the weakest in 16 modules, while *Cells* 2 and 3 are weakest in 9 and 11 modules, respectively. This uneven distribution suggests the presence of an intra-module gradient, consistent with the trends observed in Fig. 5.

### B. RESISTANCE HETEROGENEITIES

The resistance values, computed according to (7), are shown in Fig. 8 as a function of *Cell* position, at 25 °C and across all SOC levels. While the distributions exhibit comparable variance, their medians differ, with resistance increasing at lower SOC. This indicates higher internal power losses under low-charge conditions, consistent with [37]. Examining resistance as a function of *Cell* position (left-hand side) reveals a clear periodic pattern, with local minima consistently occurring at the second *Cell* within each module (i.e., the centrally positioned *Cell*). This indicates structured intra-module resistance heterogeneity. A more detailed analysis is provided in Fig. 9, which reports resistance as a function of *Cell* position at the three setpoint temperatures, aggregating all SOC levels. The centrally positioned *Cell* (position 2) forms a distinct cluster, while the outer *Cells* (positions 1 and 3) largely overlap. This separation is confirmed by the mean values, with the central *Cell* consistently exhibiting lower resistance across all temperatures (see Table 3). Additionally, resistance increases as temperature decreases and decreases as temperature increases.

The dependence of resistance on temperature is further examined in Fig. 10. For each SOC, three distinct clusters are observed, corresponding to the tested environmental temperatures (yellow: 15 °C, red: 25 °C, and brown: 35 °C). Each cluster includes all *Cells* across the modules. The measured module temperature does not exactly match the setpoint due to the transient thermal dynamics during the test, with deviations of up to +4 ° C (see Appendix III). To account for this, each data point is associated with the average module temperature measured over the eight current pulses at a given SOC. The clusters exhibit different resistance levels, with higher temperatures corresponding to lower resistance, consistent with prior findings [37]. The fitted coefficients of the resistance–temperature relationship in (8) are reported in Table 4. The resulting root mean square error (rmse) is on the order of 0.009 mΩ, i.e., two orders of magnitude smaller than the absolute resistance values, indicating high fitting

**TABLE 3.** Internal Resistance Statistics Based on the *Cell* Position Within the Module, Grouped by Setpoint Temperature

| | Internal resistance | | | |
|---|---|---|---|---|
| | mean [mΩ] | std [mΩ] | min [mΩ] | max [mΩ] |
| **@15°C** | | | | |
| *Cell* 1 | 0.2640 | 0.0083 | 0.2502 | 0.2754 |
| *Cell* 2 | 0.2482 | 0.0095 | 0.2310 | 0.2650 |
| *Cell* 3 | 0.2644 | 0.0078 | 0.2519 | 0.2795 |
| **@25°C** | | | | |
| *Cell* 1 | 0.2185 | 0.0052 | 0.2077 | 0.2253 |
| *Cell* 2 | 0.1996 | 0.0067 | 0.1858 | 0.2076 |
| *Cell* 3 | 0.2181 | 0.0063 | 0.2070 | 0.2291 |
| **@35°C** | | | | |
| *Cell* 1 | 0.1902 | 0.0027 | 0.1852 | 0.1959 |
| *Cell* 2 | 0.1736 | 0.0027 | 0.1675 | 0.1775 |
| *Cell* 3 | 0.1906 | 0.0041 | 0.1821 | 0.1971 |

**TABLE 4.** Resistance vs Temperature Fitted Model Coefficients At the Three Tested SOC Levels

| SOC level | $a_1$ | $a_2$ | $a_3$ | rmse [mΩ] |
|---|---|---|---|---|
| 90% SOC | 0.0023 | –0.0857 | 0.0001 | 0.0091 |
| 65% SOC | 0.0024 | –0.0866 | 0.0001 | 0.0092 |
| 40% SOC | 0.0024 | –0.0909 | 0.0001 | 0.0090 |

accuracy. These results highlight the strong influence of temperature on cell electrical behavior and provide a plausible explanation for the observed resistance heterogeneity within modules. In particular, the results suggest the presence of intra-module thermal gradients, where *Cell* 2 may operate at a higher temperature than *Cells* 1 and 3, leading to lower resistance. Such gradients may arise from the module layout, non-uniform heat generation, and thermal coupling among *Cells*. We note, however, that module-level (surface) temperature measurements alone are insufficient to infer (or exclude) *Cell*-level thermal gradients, as the casing may smooth out localized internal temperature variations (see Appendix III). Finally, we note that, due to the adopted voltage measurement configuration, the computed internal resistance inherently includes voltage drops across module interconnect resistances. As these contributions cannot be separated from the *Cells*' terminal voltages with the present setup, their exact impact on the reported resistance values and associated heterogeneity cannot be quantified; however, it is expected to be small. If interconnect resistances were uniform within a module, they by themselves would not explain the observed resistance heterogeneity, suggesting that geometry-dependent interconnect effects are unlikely to be the dominant factor. Nevertheless, this cannot be conclusively verified with the current measurements. Further investigation, particularly involving *Cell*-level temperature sensing and dedicated interconnect resistance

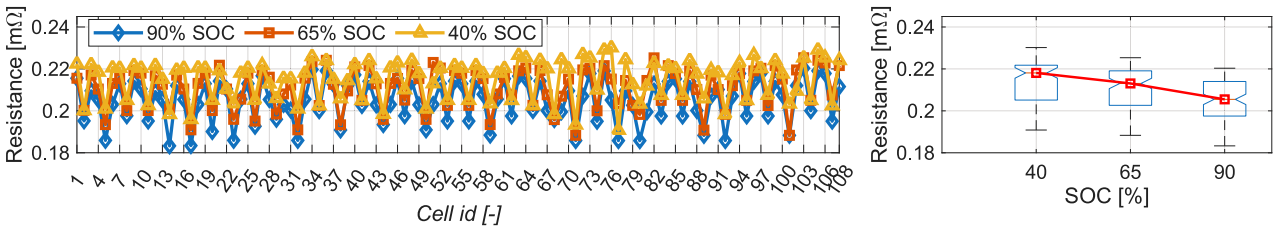


**FIGURE 8.** Left: resistances values for all 108 *Cells* in the pack, computed at 25 °C, at 40%, 65% and 90% SOC. Right: boxplots of the corresponding distributions; the red line connects the medians.

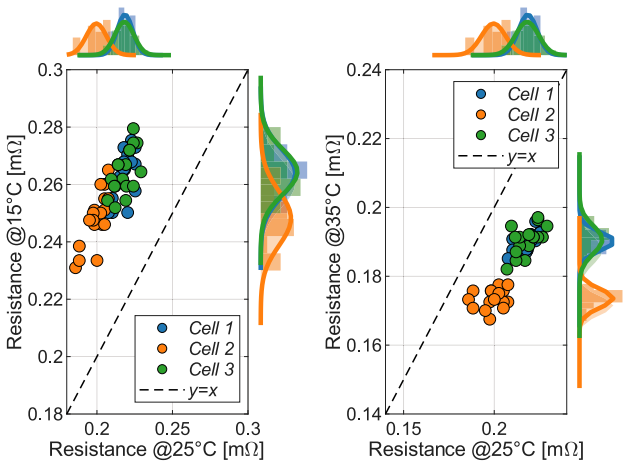


**FIGURE 9.** Comparison of resistance values at different setpoint temperatures as a function of *Cell* position within the modules (color-coded). Left: 25 °C vs. 15 °C resistance; right: 25 °C vs. 35 °C resistance. Resistance distributions by *Cell* position are also shown, with histograms fitted using Gaussian distributions.

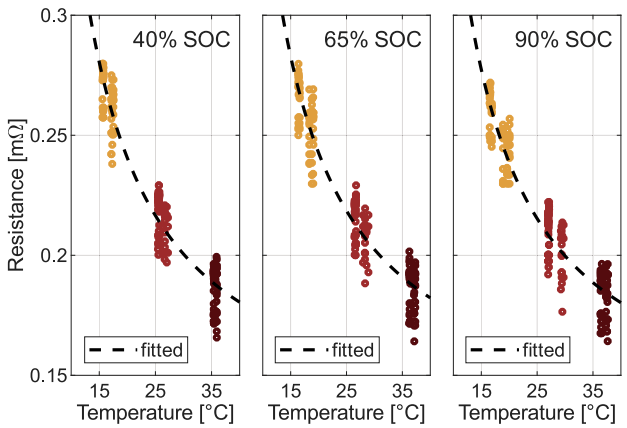


**FIGURE 10.** Scatter plot of the computed resistance values as a function of measured module temperature, across all SOC levels. The data are fitted with parabolic functions (dashed lines), according to (8).

characterization, is therefore required to fully explain this behavior.

## V. CONCLUSION

The experimental platform and methodology presented in this paper provide a non-invasive approach for cell screening during module testing. We designed and built a dedicated low-power, Monitoring & Balancing Hardware (M&BH) platform with two primary functionalities: (i) measuring and digitizing the voltages of the internal *Cells*, specifically, three voltage readings corresponding to the three series-connected *Cells*, and communicating these measurements to the battery cycler for data logging; and (ii) performing cell balancing during cycling. The balancing circuitry is critical for maintaining cell integrity during testing, preventing voltage imbalances that could compromise cell operation during module-level experiments. The collected signals are analyzed to extract quantitative metrics for assessing *Cell* performance. Specifically, capacity tests are used to determine the discharge capacity and energy of each *Cell*, and to evaluate how these quantities propagate to the module-level. In addition, HPPC tests are used to compute *Cell* internal resistance, which is characterized across different SOC values and module temperatures. The extracted metrics provide a diagnostic view of the pack's internal components, offering insights into state of health and intra-pack heterogeneity. The proposed methodology identifies distinct patterns within each module: the first *Cell* in the series is most often the weakest in terms of capacity, while the intermediate *Cell* consistently exhibits the lowest resistance. Moreover, the proposed module sensing setup enables studying trends between diagnostic indicators and operating variables such as temperature, allowing the identification and fitting of analytical relationships (e.g., resistance versus temperature). Future work will focus on direct *Cell* temperature measurements, which are expected to provide a clearer understanding of potential intra-module thermal gradients and their impact on resistance heterogeneity across *Cells*. Broadly, this work is particularly relevant for second-life applications, where accurately assessing the internal state of battery modules is essential for safe reuse and repurposing, especially in the presence of cell-to-cell heterogeneities accumulated during first-life operation. In this context, the proposed M&BH platform can serve as an accurate, non-disruptive, and safe screening tool to support module qualification and sorting prior to second-life deployment.

## ACKNOWLEDGMENT

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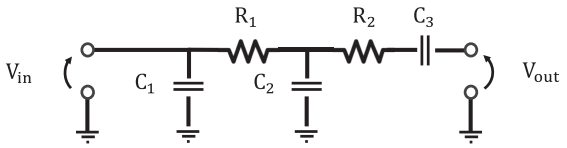


**FIGURE 11.** LP Filter scheme. The circuit comprises resistors $R_1$ and $R_2$, and capacitors $C_1$, $C_2$ and $C_3$, with parameter values listed in Table 5.

also thank P. Bosoni (pbosoni@stanford.edu) for his help with the experimental module testing activity.

## APPENDIX I
## MEASUREMENT AND DATA ACQUISITION

With reference to the M&BH schematics in Fig. 2(d), we further detail the voltage measurement pipeline.

### A. VOLTAGE SCALING AND FILTERING

The node potentials C1+, C2+, and C3+ are directly accessed through the module external connectors, defined as follows:

- C1+: potential at the positive terminal of *Cell* 1 with respect to the common ground G-;
- C2+: potential at the positive terminal of *Cell* 2 with respect to the common ground G-;
- C3+: potential at the positive terminal of *Cell* 3 with respect to the common ground G-.

Under this measurement configuration, the acquired voltages inherently include contributions from interconnect resistances between *Cells*, which cannot be decoupled from the individual *Cell* terminal voltages. However, these contributions are expected to be negligible relative to the *Cell* voltage. Each node potential is scaled 4:1 using voltage dividers formed by $R_H$ and $R_L$ (scaling factor: $\frac{R_L}{R_H+R_L} = 0.25$), ensuring compatibility with the ADC input range. To attenuate high-frequency noise and mitigate aliasing effects, a filtering network is placed between each divider output and the corresponding ADC channel, resulting in three identical low-pass filters. The filter topology is shown in Fig. 11, where $V_{in}$ denotes the voltage divider output and $V_{out}$ the voltage applied to the individual ADC input channel.

The filter comprises three functional blocks:

- input shunt capacitor ($C_1$): provides a local high-frequency return path to ground, reducing fast transients at the filter input;
- low-pass stage ($R_1, C_2$): defines the measurement bandwidth $f_{LP}$ of the filter;
- DC blocking ($R_2, C_3$): acts as an open-circuit to direct-current (DC), preventing continuous current flow into the ADC to protect the input terminal.

In the following, the cutoff frequency of the filtering network is computed by modeling $V_{in}$ as an ideal voltage source and $V_{out}$ as an open (high-impedance) circuit. Under these assumptions, the input shunt capacitor is directly driven by the input voltage and does not constitute an independent state, while the DC-blocking capacitor does not affect the output dynamics due to the absence of a current path in that branch.

**TABLE 5.** Analog Electrical Circuit Component Values

| Component | Value |
|---|---|
| Resistor $R_b$ | 67.5 Ω |
| Resistor $R_H$ | 30 kΩ |
| Resistor $R_L$ | 10 kΩ |
| Resistor $R_1$ | 3 kΩ |
| Resistor $R_2$ | 2 kΩ |
| Capacitor $C_1$ | 47 nF |
| Capacitor $C_2$ | 470 nF |
| Capacitor $C_3$ | 47 nF |

Under these assumptions, the input–output transfer function reduces to:

$$H(s) = \frac{1}{R_1 C_2 s + 1}, \tag{9}$$

with unitary gain $H(0) = 1$, time constant $\tau = R_1 C_2$, and cutoff frequency $f_{LP} = \frac{1}{2\pi\tau}$ (in Hz). Using the component values listed in Table 5, the resulting cutoff frequency is $f_{LP} = 112.9$ Hz (i.e., $\tau = 0.00141$ s). Relaxing the ideal assumptions introduces higher-order dynamics:

- a non-ideal voltage source (with a series resistance) causes the input shunt capacitor to introduce an additional pole;
- a finite output load causes $C_3$ to introduce a zero in the transfer function, leading the overall network toward a band-pass behavior.

The selected component values yield an overall filtering response consistent with standard on-board filtering stages.

### B. ADC, DIGITAL CORRECTION, AND LATENCY

The voltage measurement circuit utilizes a multi-channel ADS1115 as ADC (allowing up to four input channels), to sample the three distinct voltage channels at a frequency of 10 Hz (sampling period $T_s = 0.1$ s). Each voltage channel represents the scaled and low-passed version of the initial node potentials (C1+, C2+ and C3+). The ADC is configured with a 16-bit resolution and a programmable gain amplifier setting of ±4.096 V, which sets the maximum allowable input voltage range. In our implementation, we conservatively selected a 4:1 voltage divider ratio to remain within this limit with margin; with a maximum module voltage of 12.6 V, the ADC input reaches at most ≈ 3.15 V. For single-ended measurements, the ADS1115 provides 15 bits of usable resolution ($2^{15} = 32,768$ levels). The native quantization step for each ADC channel is therefore calculated as:

$$V_{\text{quantization,native}} = \frac{4.096\ \text{V}}{2^{15}} = 125\ \mu\text{V}.$$

The ADC communicates with the micro-controller (Raspberry Pi Pico) through a I2C line. The micro-controller performs four fundamental tasks related to voltage measurement.

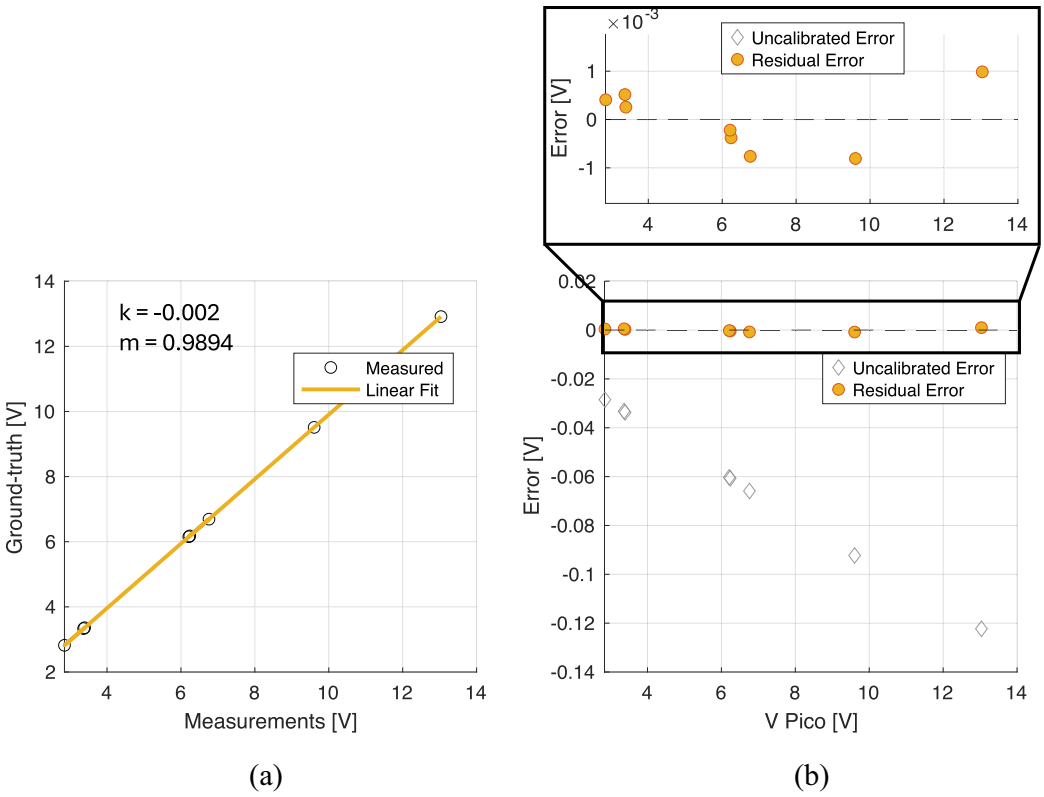


**FIGURE 12.** ADC channel calibration. Calibration results for channel 1. (a) Measured voltage from the circuit versus oscilloscope ground truth, with the best linear fit obtained via ordinary least squares. The fitted gain and bias indicate that only minor correction is required. (b) Measurement errors before and after calibration, comparing the uncalibrated error (ADC measurement vs. ground truth) and the calibration residual error. While the uncalibrated error exhibits a diverging trend, the calibrated error remains within 1 mV.

### 1) RESCALING

It rescales the potentials sampled by the ADC to their original voltage range, i.e., multiplying them by 4. In this sense, the effective voltage quantization error for each ADC channel becomes:

$$V_{\text{quantization,effective}} = 125\ \mu\text{V} \times 4 = 0.5\ \text{mV}.$$

We note that, if the hardware is adapted to modules with a higher number of series-connected *Cells*, the effective quantization error increases accordingly, since a higher voltage divider ratio is required to keep the ADC input within its allowable range.

### 2) SENSING CORRECTION

To compensate for hardware tolerances in the voltage dividers and the ADC internal gain, the data from the $j$-th ADC channel (already multiplied by 4) undergo a linear correction:

$$V_{\text{corrected}}^{\text{channel } j} = m_j \cdot V_{\text{not corrected}}^{\text{channel } j} + k_j,$$

where $m_j$ is the correction gain and $k_j$ is the correction bias. We consider a correction model for each ADC channel. The parameter pair $(m_j, k_j)$ for each channel is identified through a calibration procedure in which the ground-truth corrected voltage is provided by a high-precision digital oscilloscope. The calibration dataset is obtained by measuring the terminal voltage of randomly selected cells from our laboratory and connecting them in series to span input voltages up to 12 V. Fig. 12 shows that the linear correction model (best linear fitting using ordinary least square) yields model residuals smaller than 1 mV across the whole voltage operating range. The model fittings for the three ADC channels are reported in Table 6.

**TABLE 6.** Fitted Linear Correction Models for the ADC Channels

| ADC channel | gain $m$ [−] | bias $k$ [V] |
|---|---|---|
| First channel | 0.9894 | −0.002 |
| Second channel | 0.9910 | −0.002 |
| Third channel | 0.9907 | −0.002 |

### 3) *CELL* VOLTAGE COMPUTATION

The *Cell* voltages are computed starting from the corrected channel potentials:

- *Cell* 1 voltage: $v_1 = V_{\text{corrected}}^{\text{channel 1}}$;
- *Cell* 2 voltage: $v_2 = V_{\text{corrected}}^{\text{channel 2}} - V_{\text{corrected}}^{\text{channel 1}}$;
- *Cell* 3 voltage: $v_3 = V_{\text{corrected}}^{\text{channel 3}} - V_{\text{corrected}}^{\text{channel 2}}$.

### 4) COMMUNICATION WITH CYCLER

The *Cell* voltage values are transmitted to the cycler via the CAN bus at a sampling frequency of 10 Hz (consistent with

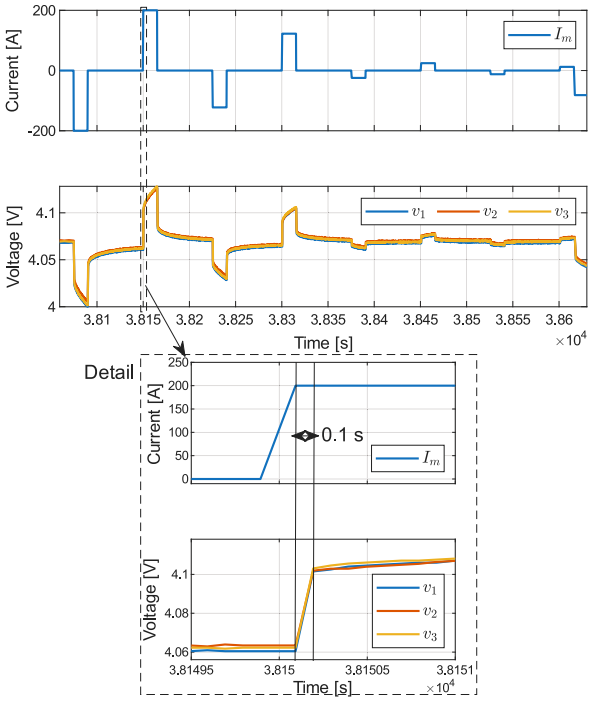


**FIGURE 13. Latency visualization. The top two plots report the module current and *Cell* voltages during the HPPC test at 90% SOC, while the bottom two plots show a zoomed-in view of the CAN communication latency. The instantaneous voltage response measured by the cycler is observed 100ms after the application of the current pulse.**

the cycler maximum logging frequency). These values are used by the cycler (i) for signal logging and (ii) to enforce current cutoffs based on prescribed *Cell* voltage thresholds during the tests (see Fig. 3 for details). Communication is bidirectional: over the same CAN link, the Arbin sends single-bit commands to the micro-controller to disable cell balancing (i.e., during discharge experiments) or enable it (i.e., to rebalance the *Cells* during CC-CV charging). Due to CAN bus communication, the voltage measurements are recorded by the battery cycler with an inherent latency observed to be approximately 100 ms. This delay, which corresponds to one sampling period $T_s$, is illustrated in Fig. 13 for an HPPC current pulse. As shown, the instantaneous voltage drop induced by the current step is registered by the cycler about 100 ms after the step change in current.

## APPENDIX II
## CELL DYNAMICS UNDER BALANCING

The electrical behavior of $j$-th *Cell* of the module is modeled using a zero-order equivalent circuit model (ECM):

$$v_j = OCV_j(SOC_j) + R_{0,j} i_j, \tag{10}$$

with $OCV_j$ open-circuit voltage, $R_{0,j}$ ohmic resistance and $i_j$ the current flowing through the *Cell*. In this work, we follow the Arbin sign convention, where the current is positive during charging; negative when discharging. The open-circuit voltage is a function of the *Cell*'s state-of-charge $SOC_j$, given by Coulomb counting:

$$\dot{SOC}_j = \frac{i_j}{Q_j}, \tag{11}$$

with $Q_j$ the *Cell*'s nominal capacity. According to the circuit schematic in Fig. 2(d), in parallel with the $j$-th *Cell* is a branch containing the switch $S_j$ and the bleeding resistor $R_b$, whose value is the same for all *Cells*. Notice that the switch position of each parallel branch is controlled by the balancing logic in (1). With reference to the $j$-th *Cell*, two scenarios arise.

*1) The Switch is Open:* In this scenario, the parallel branch is an open-circuit and no current flows through the parallel branch. Therefore, the current flowing through the *Cell* is the same as the module current:

$$\text{(open switch) } i_j = I_m, \ \forall j \in \{1, 2, 3\}. \tag{12}$$

By plugging (12) into (11), all *Cells* undergo the same SOC evolution, up to differences arising only from their individual capacities.

*2) The Switch is Closed:* In this scenario, the module current is partially diverted into the parallel branch, therefore less current flows through the *Cell*. Considering that the voltage divider resistances $R_H$ and $R_L$ are much greater than the bleeding resistance $R_b$ (consistently with the values listed in Table 5), the following relations for the $j$-th parallel branch hold (from the Kirchhoff's laws):

$$\text{(closed switch) } \begin{cases} I_m = i_j + i_{R_b} \\ v_j = v_{R_b} \\ v_{R_b} = R_b i_{R_b} \end{cases}. \tag{13}$$

Here, $v_{R_b}$ is the voltage drop across the bleeding resistor, and $i_{R_b}$ the current flowing through the parallel branch. By incorporating (10)–(11), (13), we obtain the following SOC dynamic equation for the $j$-th *Cell:*

$$\dot{SOC}_j = \frac{R_b}{Q_j(R_{0,j} + R_b)} I_m - \frac{OCV_j(SOC_j)}{Q_j(R_{0,j} + R_b)}. \tag{14}$$

Therefore, each *Cell*'s SOC can be controlled independently via the closing of the corresponding parallel switch. Two key observations are made on the value of $R_b$:

- given a constant module current, if the bleeding resistance value is exactly equal to $\frac{OCV_j(SOC_j)}{I_m}$, then no current flows through the $j$-th *Cell*, effectively freezing its state-of-charge, i.e., $\dot{SOC}_j = 0$;
- in the case of bleeding resistance with value $R_b \gg R_{0,j}$, only a very small fraction of the module current is diverted into the parallel branch. Consequently, the evolution of the *Cell*'s SOC is only marginally slowed down with balancing.

Generally, $R_b$ may be selected based on the desired SOC dynamics under balancing. In this context, $R_b$ serves as a design parameter: the lower its value, the smaller the *Cell* charging rate.

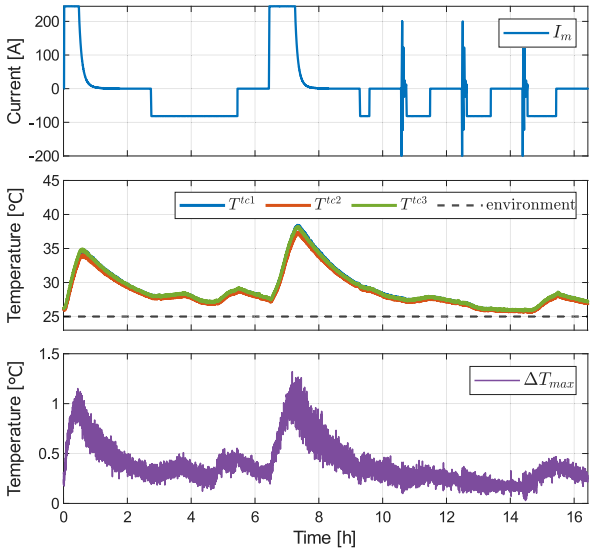


**FIGURE 14.** Top: module current over the entire test. Middle: thermocouple temperatures $T^{tc1}$, $T^{tc2}$, $T^{tc3}$ (solid lines) with environmental setpoint (dashed). Bottom: maximum surface temperature difference $\Delta T_{max}$.

## APPENDIX III
## TEMPERATURE INSTRUMENTATION

Fig. 2(b) shows the module instrumented with three Type-T thermocouples (model 5SRTC-TT-T) placed near the positive terminal, negative terminal, and center of the upper surface. The corresponding temperature traces ($T^{tc1}$, $T^{tc2}$, $T^{tc3}$) for module no.29 are reported in Fig. 14 at a chamber setpoint of 25 °C. The module starts at thermal equilibrium, and its surface temperature increases with current, peaking during 1 C charging. During rest periods, the temperature relaxes toward the setpoint but does not fully return to equilibrium due to limited rest duration. The three thermocouples report consistent readings throughout the test. Defining the maximum module surface temperature difference as:

$$\Delta T_{\max} = \max\left(T^{tc1}, T^{tc2}, T^{tc3}\right) - \min\left(T^{tc1}, T^{tc2}, T^{tc3}\right), \tag{15}$$

the bottom subplot of Fig. 14 shows that $\Delta T_{\max}$ reaches $\sim$1 °C during 1C charge and remains below 0.5 °C during the C/3 test and HPPC pulses. This indicates weak thermal gradients across the module surface.[1]

Despite the observed *Cell* internal resistance heterogeneity, the small $\Delta T_{\max}$ alone does not explain the pattern in Fig. 8. Surface measurements may not capture internal *Cell* temperatures, as the casing can smooth localized gradients. Therefore, intra-module thermal gradients at the *Cell*-level cannot be excluded based on surface data alone. Further investigation should rely on direct *Cell*-level temperature measurements.

[1]Differences below 1 °C are within the ±1 °C thermocouple accuracy [38].

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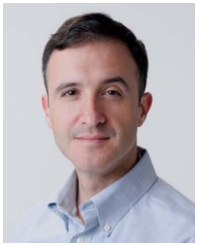
**GABRIELE MARINI** was born in Penne, Italy. He received the Ph.D. degree in information technology from Politecnico di Milano, Milan, Italy, in 2024. Since 2024, he has been a Postdoctoral Researcher with the Department of Energy Science & Engineering, Stanford University, Stanford, CA, USA. He has a background in systems, control and optimization theory. His research interests include state-of-health estimation of lithium-ion batteries, digital twins of EV battery packs, and parameter identification for battery electrochemical models. He has worked on control and estimation for transportation systems and high-performance vehicles.

**ALESSANDRO COLOMBO** was born in Busto Arsizio, Italy. He received the B.Sc. and M.SC. degrees in automation and control engineering from Politecnico di Milano, Milan, Italy, in 2020 and 2022, respectively. He is currently working toward the Ph.D. degree in information technology with Politecnico di Milano. From January to June 2024, he was a Visiting Student with the Energy Science and Engineering Department Stanford University, where the work described in this paper took place.

**ANDREA LANUBILE** was born in Lecce, Italy. He received the B.Sc. and M.Sc. degrees in automation and control engineering from Politecnico di Milano, Milan, Italy. Since 2024, he has been working toward the Ph.D. degree with Stanford Energy Control Lab, Stanford University, Stanford, CA, USA. His research interests include state-of-health estimation of lithium-ion batteries, with a particular focus on identifying and tracking heterogeneities in battery packs.



**WILLIAM A. PAXTON** was born in New York, NY, USA. He received the Ph.D. degree in materials science and engineering from Rutgers University, New Brunswick, NJ, USA. He was an Electrification and Materials-Engineering with Ford Motor Company. He is currently a Senior Staff Scientist and Project Lead with Volkswagen Group's Innovation Center California, Belmont, CA, USA, where he leads research on electric-vehicle energy systems and advanced battery diagnostics. He has authored publications spanning battery diagnostics, electrochemical materials, and electric-vehicle energy systems. His research interests include lithium-ion state-of-health modeling, second-life evaluation, and the integration of EV battery assets with grid and charging-infrastructure environments.

**SIMONA ONORI** (Fellow, IEEE) received the Ph.D. degree in control engineering from the University of Rome Tor Vergata, Rome, Italy. She is currently an Associate Professor of energy science and engineering with Stanford University, Stanford, CA, USA, where she directs the Stanford Energy Control Laboratory, holds a courtesy appointment in electrical engineering, and is a Senior Fellow of the Precourt Institute for Energy. She has authored more than 200 publications and holds multiple patents in battery management and energy storage. Her research interests include advances the modeling, estimation, and optimization of electrochemical energy systems, lithium-ion batteries, fuel cells, and hybrid electric powertrains, with an emphasis on bridging fundamental electrochemistry with advanced control and data-driven methods. She is a fellow of SAE International, and serves as the Editor-in-Chief of *SAE International Journal of Electrified Vehicles*. Her work has been recognized with several major awards for contributions to energy systems and electrification.